Page 1

Descriptives 1.Datos Digital Systems 1 Tutorial - Student Information Subject **Digital Systems 1** Matter M5. ELECTRONIC Department responsible **Electronic Engineering ECTS credits** 4.5 Character Compulsory Degree Diploma in Engineering Technology and Services Telecommunication Course 3rd Specialty N / AAcademic year 2011-2012 Semester in which imparts First Language in which imparts Castilian Website http://moodle.upm.es/titulaciones/oficiales

2.Profesorado NAME **OFFICE** E-mail Carlos Carreras Vaquer C-230 carreras@die.upm.es Ricardo Cordoba Herralde B-108 cordoba@die.upm.es María Jesús Carballo Ledesma C-201A mledesma@die.upm.es Juan Manuel Montero Martinez B-110 juancho@die.upm.es

Previous 3.Conocimientos required to continue normally the subject Subjects overcome

Other results learning necessary

• Programming

• Fundamentals of telematics systems

• Digital Electronics

4.

Page 3

Learning Objectives. Powers assigned to the subject and level of **ACQUISITION** Code Competition Level CG1-CG5 All subjects contribute Curriculum greater or lesser extent to the achievement of the general skills of the graduate profile. CG6 Use of English. 1 CG9 Use of Information Technologies and Communications. 2 CG12 Organization and planning 1 CECT1 Ability to independently learn new knowledge and techniques for the design, development or operation of systems and services telecommunication. 1 CECT2 Ability to use communication applications and computer (office automation, databases, advanced calculus, project management, visualization, etc..) to support the development and operation of networks, services and applications telecommunications and electronics. 2 CECT3 Ability to use computer tools

search library resources or information related to telecommunications and electronics.

1

CECT6

Ability to design, deploy, organize and manage networks, systems, services and infrastructure telecommunication in residential settings (home, city and digital communities), corporate and institutional responsible for their implementation and improvement continuous and know their economic and social impact 1

CECT9

Capacity for analysis and design of circuits combinational and sequential, synchronous and asynchronous, and use of microprocessors and integrated circuits. 2

CECT11

Ability to use different energy sources and especially solar photovoltaic and thermal, as well as fundamentals of electrical engineering and electronics power.

1

LEGEND: Acquisition Level 1: Basic Acquisition level 2: Middle Acquisition Level 3: Advanced LEARNING OUTCOMES OF THE COURSE Codi go Learning result Competencias associated Level of acquired position RA1 Ability to analyze and design electronic circuits, both analog and digital. CECT6 CECT9 1 RA2 Understanding the structure of computers, microprocessors and microcontrollers and their programming languages, knowledge of Peripheral devices and input / output. CECT1

CECT2 CG6 CG9 CG12 3 RA3 Ability to design systems based on microprocessors. CECT3 CECT6 CECT9 CG12 2 RA4 Knowledge of the mechanisms and timing management interrupts. CECT1 CECT3 CECT9 CG6 CG12 3 RA5 Knowledge of implementation techniques, debugging and testing of systems based on microprocessors. CECT1 CECT2 CECT9 CG6 CG9 2 RA6 Ability to integrate analog and subsystems digital microprocessor-based systems. CECT3 CECT6 CECT9 CG12 2

Page 5

LEARNING OUTCOMES OF THE COURSE Codi go Learning result Competencias associated Level of acquired position RA7 Knowledge and ability to source selection energy, batteries and inverters. CECT1 CECT11 1 LEGEND: Acquisition Level 1: Knowledge descriptive Acquisition Level 2: Comprehension / Application Acquisition Level 3: Analysis / Synthesis / Implementation 5. System evaluation of the subject **ACHIEVEMENT INDICATORS** Ref Indicator Related do with RA **I**1 Knowing the basics of a system microcontroller (microcontroller internal registers and buses, functional units, and the units for address calculation), its architecture and functional structure and the instruction execution process. Identify characteristics and applications of different ranges and types processors and memories. RA1 RA2 RA3 I2 Analysis and assembly language programming, including detailed knowledge of assembler directives, the programming model and instruction set of a microprocessor. RA2 RA3 RA5 I3 Understand the organization of data in memory modes addressing and the operation of the battery in a system microprocessor. RA2

ACHIEVEMENT INDICATORS Ref Indicator Related do with RA I4

Know the different types of peripherals in a microcontroller, groups of terminals, the configuration transfer by the external bus access and the concept of Direct Memory. Analyze analog and digital circuits as basic peripherals that connect to external bus. Know and set the power management system of a microprocessor.

RA1 RA2

RA4

RA5

RA7

I5

Designing the memory map of a microprocessor system, configure the memory system and implement the map memory using hardware circuitry or programming Software.

RA2

RA3

I6

Knowing the types of exceptions in a processor, the processing the same, the distinction between exceptions and interruptions, the different types of interruptions and concepts of priority and interrupt mask.

Analyze and configure the operation of the interrupt a microprocessor programmed to analyze and routines attention thereto.

RA4

I7

Knowing the characteristics of parallel communications and in series with a microcontroller, as well as key connection and communication standards. Analyze and schedule the use of ports in parallel and in series is one when connected to individual peripherals including implementation of protocols from the program

implementation of protocols from the program.

RA2

RA3

I8

Knowing the characteristics of a timer module, being able to analyze your performance and set for capture input and output comparisons.

Knowing the operation and configuration of a modulator

PWM pulse width, and their application to the

speed control of DC motors.

RA2

RA3

I9

Knowing the internal structure and features of static and dynamic memories as well as the concept of caches. Designing memories composed of several memory chips to get the word size or from desired capacity available chips commercially. RA3 I10 Analysing and designing complete systems based on the use of microprocessors RA3 RA6

Page 7

Summative Brief description of the assessable activities Time **Place** Weight in the calif. **Evaluation issues 1-5** 26/11/2012 A designate 35 Assessment items 6, 7 and integration knowledge Call official A designate 50 Continuous assessment of participation and problems posed in class Weeks 1 to 15 Classroom 15 **Total: 100% Qualification Criteria**

In ordinary exam, students will be assessed by continuous assessment. However, students who wish may be evaluated by a single final test so long as expressed through formalized in writing ETSI Telecommunications registration and to the Director of the Department of Electronic Engineering or before October 5, 2012 (end of week 5). The presentation of this paper constitute a waiver automatic continuous assessment. **REGULAR CALL: CONTINUOUS ASSESSMENT METHOD** The course will be approved when getting a grade greater than or equal to 5

points on a total of 10. This rating is the sum of the ratings

for the various assessment activities, with the following weights:

- Evaluation issues 1-5 (partial): 35%
- Assessment items 6, 7 and integration (official announcement): 50%
- Participation and delivery problems in class: 15%

The evaluation of the issues 1-5 will be released in case of obtaining a rating N1a equal or greater than 4 points. Should you get less than 4 points or want up note, the student must be submitted to the recovery in the official examination, obtaining N1b note. The final note of the partial examination in such cases is calculated

as N1a + N1b * 0.2 * 0.8.

REGULAR CALL: EVALUATION BY A SINGLE TEST FINAL

The 100% of qualifying students who submit the referral is written above awarded based on a single test at the end to celebrate the official announcement.

EXTRAORDINARY

The evaluation of the subject in his extraordinary call will be made by one final test to be held on a date determined by Head of Studies, with Regardless of the option chosen in the ordinary call.

Page 8

6. Content and Learning Activities SPECIFIC CONTENT Block / Theme / Chapter Paragraph **Indicators** Related two **Topic 1: The** system microprocessor 1.1 Elements of a microprocessor system. System microprocessor. Applications. Functional structure. The Central Unit Process. Executing a command. The main memory. Peripherals. The connecting lines. The memory map. **1.2 The microprocessor market.** Types of processors and memories. Ranges processor. The market semiconductors. The market for microcontrollers. The family ColdFire. The ColdFire MCF5272. **I**1 Item 2: **Programming** Family ColdFire 2.1 Programming in assembler. Components of a program. Assembly language syntax. Assembler directives. The assembly process. Development and debugging programs. 2.2 The ColdFire programming model. Model programming. Execution modes. Organization in memory. Stack. Addressing Modes. Access to data structures.

2.3 The ColdFire instruction set: data. Movement data. Data transfer with the stack. Handling bits. Click lógincas. Shift Instructions. Instructions arithmetic. Extended Arithmetic. Compare and test instructions. 2.4 The ColdFire instruction set: control. Control agenda. Unconditional jumps. Subroutines and parameter passing by the stack. Conditional statements. Mode Control System user and supervisor mode. I2 I3 Item 3: Architecture hardware **MCF5272** 3.1 System Architecture. MCF5272 Block Diagram. The ColdFire core. Pipelined architecture. Instruction Timing. MCF5272 local memory. The system integration module (SIM). MCF5272 Modules. MCF5272 terminals. The bus external. Transfer Modes. Power circuits, clock and reset. Booting. **3.2 Configuration of the memory system.** System memory the MCF5272. Setting internal devices. Access external devices. Chip select signals. The module MCF5272 chip selection. Programming a map memory. Direct Memory Access (DMA).

I1

I4 I5

Page 9

SPECIFIC CONTENT Block / Theme / Chapter Paragraph **Indicators** Related two Item 4: **Exceptions** system microprocessor **4.1 Exceptions.** Definition and exception types. Vector table exception. Setting the vector table. Priority between exceptions. The exception processing. Subroutines versus exceptions. Reset error and stopping the system bus. 4.2 Interrupts. Vectored interrupts and autovectorizadas. Probe against interruptions. Priorities and masking. MCF5272 interrupt sources. The interrupt controller the MCF5272. Interrupt configuration. 4.3 Management of consumption. The power management module of MCF5272. Low-power modes. Setup for low power consumption.

I4

I6

Item 5:

In / Out

into the system

microprocessor

5.1 Input / Output. Interfaces and peripheral input / output. Types communication. Coding Standards symbols. Types parallel communication. MCF5272 parallel ports. Control a matrix keyboard. Handling an LCD display. Communication asynchronous serial. Circuits and asynchronous communication errors. Synchronous serial communication. Serial communication standards. The simplified MCF5272 UART module.

I7

I10

Item 6:

Modules

timing

into the system

microprocessor

Programmable Timers 6.1. Elements of a timer.

Resolution and range. The input capture: circuits and applications. The output compared: circuits and applications. The timer module the MCF5272. Setting the input capture. Configuration Output of the comparison. Combination and input capture output comparison.

6.2 pulse width modulation. Modulation PWM.

Block diagram of a PWM modulator. The PWM module MCF5272. PWM module configuration. Application to the control of speed of a DC motor.

I8

I10 Item 7:

Memories in the

system

microprocessor

7.1 Memory VLSI integrated. Types nonvolatile memories. Type volatile memory. The memory chip. Memory hierarchy SROM and RAM. Expanding word size and number of words.

7.2 Dynamic Memory. DRAM. Entries in memoriesDRAM. Structure of a DRAM memory. Elements in memoriesDRAM. The refresh process. DRAM controllers.I9

7. Brief description of the modalities organizational used and methods teaching employees

Lectures

It presents the concepts, language programming, modules and devices to be used in Digital Systems.

CLASSES

PROBLEMS

Resolve practical problems related to the analysis of complete system based on a microprocessor and also part of the same design. These problems always offer the student prior to the resolved as personal work. Classes are participatory with the possibility of continuous assessment of students in the classroom. **CLASSES**

DEMONSTRATIVE

During this session (only one in the entire course), which performed in the laboratory, students are presented with a case Practical use of the development environment microprocessor. Each student must submit a small summary / test on it.

WORK

Al along the course, some of the problems to be resolved by the student as part of their personal work must be submitted and posted as part of its ongoing evaluation.

TUTORING

Are performed in accordance with regulations

11

8. Teaching resources TEACHING RESOURCES REFERENCES

• C. Carreras et al., Digital System Design with ColdFire microcontroller 5272, ETSI Telecommunications. • R. San Segundo et al., Introduction to Systems Digital MCF5272 microcontroller, Ed Marcombo. • A Clements, Microprocessor Systems Design. 68000 Hardware, Software and Interfacing, PWS-Kent Publishing. • J. Septien et al., Meet the MC68000. Language assembler: Connecting and programming interfaces, Ed Synthesis. • Freescale ColdFire Family Programmer's Reference Manual, www.freescale.com • Freescale ColdFire 2/2M Version Processor Core User's Manual, www.freescale.com • Freescale ColdFire MCF5272 Integrated Microprocessor User's Manual, www.freescale.com **WEB RESOURCES** Website of the subject http://moodle.upm.es/titulaciones/oficiales

EQUIPMENT

Classroom: Assigned by Head of Studies Digital Systems Laboratory B-043

12 9. Work schedule of the course Week **Classroom Activities** Activities Laboratory **Individual Work** Workgroups Activities **Evaluation** Others Week 1 (5 h) • Presentation (0.5 h) • Item 1.1 (2 h) • Topic 1.2 (0.5 h) • Study and review theory of previous concepts (2 h) • Possibility continuous assessment Classroom Week 2 (5 h) • Topic 2.1 (1.5 h) • Item 2.2 (1.5 h) • Study of theory and Examples (2 h) • Possibility continuous assessment Classroom Week 3 (9 h) • Topic 2.3 (2h) • Item 2.4 (1 h) • Demonstration environment development (1.5 h) • Study of theory and examples (1.5 h) Troubleshooting proposed (2 h) •

Preparation of the test on demonstration in laboratory (1 h) • Demonstration the laboratory Groups of three • Possibility continuous assessment Classroom Week 4 (5 h) • Problems (2 h) • Item 3.1 (1 h) • Study of theory (1 h) • Review of problems proposed (1 h) • Possibility continuous assessment Classroom • Delivery of test on demonstration in laboratory

13

Week **Classroom Activities** Activities Laboratory Individual Work Workgroups Activities Evaluation Others Week 5 (8 h) • Item 3.1 (1 h) • Item 3.2 (1 h) • Problems (1 h) • Study of theory (2 h) • Troubleshooting proposed (3 h) • Possibility continuous assessment Classroom Week 6 (5 h) • Problems (2 h) • Item 4.1 (1 h) • Review of problems

proposed (2 h) • Possibility continuous assessment Classroom Week 7 (7 h) • Item 4.2 (1.5 h) • Item 4.3 (1 h) • Problems (0.5 h) • Study of theory and Examples (2 h) • Troubleshooting proposed (2h) • Possibility continuous assessment Classroom Week 8 (6 h) • Problems (2 h) • Theme 5 (1 h) • Study of theory and Examples (1 h) • Troubleshooting proposed (2h) • Possibility continuous assessment Classroom Week 9 (7 hours) • Item 5 (2h) • Problems (1 h) • Review of problems proposed (2 h) • Resolution of problems deliver Item 4 (2 h)• Possible continuous assessment Classroom Week 10 (8 hours) • Problems (2.5 h) • Problems delivered (0.5 h) • Study of theory and Examples (2 h) • Troubleshooting proposed (3 h) • Possibility continuous assessment Classroom

• Delivery of problems Proposed Item 4

14

Week **Classroom Activities** Activities Laboratory Individual Work Workgroups Activities Evaluation Others Week 11 (9 hours) • Item 6.1 (2.5 h) • Item 6.2 (0.5 h) • Review of problems proposed (2 h) • Resolution of problems deliver Item 5 (2 h) • Test Preparation part (2 h) • Possibility continuous assessment Classroom Week 12 (12 h) • Problems delivered (0.5 h)• Problems (2.5 h) • Study of theory and Examples (2 h) • Troubleshooting proposed (3 h) • Test Preparation part (4 h) • Possibility continuous assessment Classroom • Delivery of problems proposed Item 5 Week 13 (8 h) • Problems (1.5 h) • Resolution of the review partial (0.5 h)

• Item 7.1 (1 h) • Review of problems proposed (1.5 h)• Resolution of problems deliver Item 6 (2 h) • Solution in Common midterm exam • Midterm Exam (11/26/2012) (1.5 h) • Possibility continuous assessment Classroom Week 14 (8 h) • Item 7.2 (1 h) • Problems handed (1 h) • Problems (1 h) • Study of theory and Examples (2 h) • Troubleshooting proposed (3 h) • Possibility continuous assessment Classroom • Delivery of problems proposed Item 6

15

Week **Classroom Activities** Activities Laboratory Individual Work Workgroups Activities Evaluation Others Week 15 (8 h) • Problems (3 h) • Review of problems proposed (1.5 h) • Exam Preparation end (3.5 h) • Possibility continuous assessment

Classroom Period before examination final (10 h) • Exam Preparation final (7 pm) • Final Evaluation (3 h) Note: For each activity specified in hours dedication to the student involved. The weeks are outlined effective teaching (not calendar weeks

16