ÁNGEL FERNÁNDEZ HERRERO

Laboratory of Electronic Circuits and Systems (LCSE)

Course Description

Departamento de
Ingeniería
Electrónica

Universidad Politécnica de Madrid

Máster Oficial en Ingeniería
de Sistemas Electrónicos

www.die.upm.es

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Laboratory of Electronic Circuits and Systems (LCSE 1)

Semester: 1

Number of credits: 4 (laboratory)

Type: mandatory

Objectives

The knowledge of digital electronics to the practical design of a digital medium of medi-um-high complexity is applied in this course. For this, it has to be able to reach a physical imple-mentation from functional specifications following the methodology of synchronous digi-tal circuit design.

The emphasis of the laboratory is made in the use of CAD tools to design complex digital cir-cuits using the VHDL description hardware language. By taking advantage of this scenar-io, other important practical issues will be also covered related to the design of complex digital systems. Validation of development is an important task to be performed by simulation, as in professional environments.

Throughout the course the student has to perform several practices by applying the different phases of a classic methodology of design:

1. Study of design CAD tools

2. VHDL specification and simulation techniques

3. Synthesis and implementation over FPGA

More specifically, the goals of the course can be described as follows:

− Experience in the development of complex digital systems

− Develop the analysis ability of a specification

− Use professional tools for synthesis and digital simulation

− Understand the importance of synchronous digital systems

− Learn techniques for debugging hardware systems through simulation

− Properly plan the developing stages of a complex system

− Address all phases of development until the final test in a real FPGA

Program

Topic 1: The VHDL
Levels of abstraction
Data types and subtypes, conversions
Constants, signals and variables, attributes
Assignments, operators
Entities, ports and generics
Architectures, concurrent sentences
Processes and sensitivity lists, sequential statements
Reuse of components, packages and libraries
Test benches, wait and after

Topic 2: Practical considerations for design and simulation-verification
State machine description
Concept synthesizable code
Synthesis common Inferences
Combinational and sequential processes
Timing and simulation
Files restrictions

Topic 3: Common mistakes in the use of VHDL
Incomplete lists sensitivity
Appearance of latches
Combinational loops
Assigning multiple signal
Use of signals and variables
Token Initialization

Practice I: consists of guided exercises with the purpose of introducing the language VHDL hardware description of and familiar with software development tools, plus the design of a small module complexity that then become part of Practice II system.

Practice II: Design of specifications for a complete digital electronic system complexity average.

Bibliography

The teaching materials consist of:

1. Statement of the proposed practices.
2. Slides used in the classes taught.
3. VHDL code required for practices.

All material becomes accessible through the course's website after the corresponding lec-tures are given.

A particular book is not followed, but a number of them are recommended for reference, all of them available at the school library:

- Sundar Rajan, Essential VHDL: RTL Synthesis Done Right, 1998.
- Jean-Michel Bergé, VHDL Designer's Reference, Kluwer Academic Publishers, 1992.
- Roger Lipsett, Carl Schaefer, VHDL: Hardware Description and Design, Kluwer Academic Publishers, 1989.
- Stefan Sjoholm, Lennart Lindh, VHDL for Designers, Prentice Hall, 1997.
- Peter J. Ashenden, The Designer's Guide to VHDL, Morgan Kaufmann Publishers, 2nd Edition, 2002.

MATERIAL RESOURCES AVAILABLE

The laboratory currently consists of four full development positions connected to the local network. Each is equipped with the following elements:

1. PC Computer with high resolution screen
2. XESS XSB-300E prototyping board with FPGA Xilinx Spartan 2S
3. Linux operating system Ubuntu 8.04
4. Software for synthesis Xilinx ISE 9.1i
5. Software for simulation Mentor ModelSim 6.2g

Teaching Methodology

The subject is raised on the completion of two practices of increasing complexity, for which students are grouped in pairs. Each pair is assigned a preferred assistance shift with a duration of 3 hours.

I Practice addresses VHDL language learning and introduction to simulation and synthesis tools. It is a guided practice that is done so that students become familiar with the working environment and gain an initial understanding of VHDL. To this end, we propose several simple exercises that will serve as a model for the description of the essential elements of digital design using VHDL, including combinational and sequential logic. In a UL-thymus exercise, the student must VHDL code itself, deepening also on the results of the synthesis processes performed. This exercise should be made to work in protipado plate.

In Practice II involves the development of a medium complexity digital system from given specifications following a standard methodology PBL (Problem-Based Learning), so that the student claim your training according to the needs that arise in solve the problem. The student must generate the VHDL code of the building blocks of the system and the necessary stimulus for the proper design verification.

Additionally, on the topics taught classes that have critical impact on the system design, such as timing, design state machines or access to bu months. Classes also are taught introduction to the tools and language VHDL.

Evaluation

The aim of the proposed practice I is to familiarize students with development tools and to discover the special features of digital hardware specification through high-level languages, since it is intrinsically different from the software programming, which they are very used to.

In this sense, they are asked to hand in the answers to the issues raised in Exercises 1 through 6 as well as the generated code for Exercise 7, which will be analyzed by teachers to determine the degree of competence acquired. Then, they will meet with the students to discuss the difficulties and correct deficiencies in the work methods and specification in order to facilitate the approach of Practice II.

The ultimate goal of the course consists of the implementation of the proposed system in Practice II, reaching, if possible, the real testing on the prototyping board. Thus, the emphasis is more on the development of the specification skills, simulation and debugging, and less on the generation of documentation. Since the number of students is not very high, teachers carry out a very close monitoring of their work.

At the end of the course the students are asked to hand in all the generated code and a brief re-port of the work done in Practice II, including the following information:

- Decisions made on the chosen architecture
- Differences with the proposed scheme and justification
- Difficulties encountered and their solution
- Degree of achievement of the final prototype

The final evaluation is based on the information in the report together with the results of a practical oral examination that takes place between a teacher and each lab Group, where the students must demonstrate:

- Their knowledge about the system developed
- The achievement grade in it
- Their proficiency in the use of tools and methodologies

The teacher also observes the ability of the students to communicate technical information, knowledge, justifications, etc. effectively and concisely and to answer the questions they are posed.

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